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FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
SAVLA, ARPAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,776	KUMAR, ALOK	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

In view of the Appeal Brief filed on May 8, 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing at the end of this action.

OBJECTIONS

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Nowhere in the specification does it disclose a "computer

program product" or a "machine-readable medium", much less a "computer program product, tangibly embodied in a machine-readable medium."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 9-11, 19-21, 24, 27, 30, and 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Calvignac et al. (U.S Patent Application Publication 2003/00448785) (hereinafter "Calvignac").

4. As per claims 1 and 11, Calvignac discloses a method comprising:

allocating a memory entry in a memory device to executable instructions to be executed on a multithreaded engine included in a packet processor (paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, elements 103 and 211). *It should be noted that computer program product in claims 11-20 executes the exact same functions as the methods in claims 1-10. Therefore, any references that teach claims 1-10 also teach the corresponding claims 11-20. It should also be noted that an "entry" within "CAM 211" is analogous to the "memory entry in a memory device", the "actions" within*

a "data structure entry" in "data structure memory 206" are analogous to the "executable instructions", "packet processor 103" is analogous to the "multithreaded engine", and "blade 102" is analogous to the "packet processor."

and including a unique identifier assigned to the executable instructions in a portion of the memory entry (paragraph 0029). *It should be noted that the "entry number" is analogous to the "unique identifier."*

5. **As per claims 21 and 24**, Calvignac discloses a memory manager/system comprising:

a process/packet processor (paragraph 0010; Fig. 1, element 102) to:

allocate a memory entry in a memory device to executable instructions to be executed on a multithreaded engine included in a packet processor (paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, elements 103 and 211). *See the citation note for the similar limitation in claims 1 and 11 above.*

and include a unique identifier assigned to the executable instructions in a portion of the memory entry (paragraph 0029). *See the citation note for the similar limitation in claims 1 and 11 above.*

6. **As per claim 27**, Calvignac discloses a network forwarding device comprising:

an input port for receiving packets (paragraph 0018; Fig. 1, element 100);

an output for delivering the received packets (paragraph 0018; Fig. 1, element 104);

a network processor (paragraph 0010; Fig. 1, element 102) to:

allocate a memory entry in a memory device to executable instructions to be executed on a multithreaded engine included in a packet processor (paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, elements 103 and 211). *See the citation note for the similar limitation in claims 1 and 11 above.*

and include a unique identifier assigned to the executable instructions in a portion of the memory entry (paragraph 0029). *See the citation note for the similar limitation in claims 1 and 11 above.*

7. **As per claim 30**, Calvignac discloses a method comprising:

allocating a content-addressable-memory (CAM) entry to an executable microblock to be executed on a multithreaded microengine included in a network processor (paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, elements 103 and 211). *It should also be noted that an "entry" within "CAM 211" is analogous to the "CAM entry", the "actions" within a "data structure entry" in "data structure memory 206" are analogous to the "executable microblock", "packet processor 103" is analogous to the "multithreaded microengine", and "blade 102" is analogous to the "network processor."*

and including a unique identifier assigned to the executable microblock in a portion of the CAM entry (paragraph 0029). *See the citation note for the similar limitation in claims 1 and 11 above.*

8. **As per claims 9 and 19**, Calvignac discloses the unique identifier includes four bits (paragraph 0030).

9. **As per claims 10 and 20**, Calvignac discloses the memory entry identifies a location in a local memory included in the multithreaded engine of the packet processor (paragraph 0029; Fig. 2, element 206). *It should be noted that "data structure memory 206" is analogous to the "local memory."*

10. **As per claims 33-37**, Calvignac discloses the memory entry comprises a content-addressable memory entry (paragraph 0029; Fig. 2, element 211).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3, 6-8, 13, 16-18, 23, 26, 29, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Kloth et al. (U.S. Patent 6,570,877) (hereinafter "Kloth").

13. **As per claims 3 and 13**, Calvignac discloses a memory entry for thread use (paragraphs 0021 and 0026).

Calvignac does not disclose maintaining a bit to represent availability of the memory entry.

Kloth discloses maintaining a bit to represent availability of the memory entry (col. 6, lines 6-16; Table 1).

Calvignac and Kloth are analogous art because they are from the same field of endeavor, that being network processing using CAMs.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Kloth's dirty bit to Calvignac's CAM because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of allowing the packet processor to quickly determine which entries in the CAM are available for use.

Therefore, it would have been obvious to combine Calvignac and Kloth for the benefit of obtaining the invention as specified in claims 3 and 13.

14. **As per claims 6 and 16**, the combination of Calvignac/Kloth discloses maintaining the bit includes clearing the bit to represent availability of the memory entry for thread use (Kloth, col. 6, lines 6-16; Table 1; Calvignac, paragraphs 0021 and 0026).

However, active high (1) and active low (0) are art-recognized equivalents in the computer arts insomuch as it is immaterial whether a state bit is high (setting the bit) or low (clearing the bit) in one state so long as the bit is the opposite level in the opposite state. Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to substitute Kloth's dirty bit being set to 0 when the entry is available with a dirty bit that is instead set to 1 when the entry is available.

Therefore, it would have been obvious to modify Calvignac/Kloth for the benefit of obtaining the invention as specified in claims 6 and 16.

15. **As per claims 7 and 17**, the combination of Calvignac/Kloth discloses maintaining the bit includes setting the bit to represent unavailability of the memory entry for thread use (Kloth, col. 6, lines 6-16; Table 1; Calvignac, paragraphs 0021 and 0026).

However, active high (1) and active low (0) are art-recognized equivalents in the computer arts insomuch as it is immaterial whether a state bit is high (setting the bit) or low (clearing the bit) in one state so long as the bit is the opposite level in the opposite state. Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to substitute Kloth's dirty bit being set to 1 when the entry is unavailable with a dirty bit that is instead set to 0 when the entry is unavailable.

Therefore, it would have been obvious to modify Calvignac/Kloth for the benefit of obtaining the invention as specified in claims 7 and 17.

16. **As per claims 8 and 18**, the combination of Calvignac/Kloth discloses checking the bit to determine the availability of the memory entry for thread use (Kloth, col. 6, lines 47-55; Calvignac, paragraphs 0021 and 0026).

17. **As per claim 23**, the combination of Calvignac/Kloth discloses a process to maintain a bit to represent availability of the memory entry (Kloth, col. 6, lines 6-16; Table 1; Calvignac, paragraphs 0021 and 0026). *See the rejection of claims 3 and 13 above.*

18. **As per claim 26**, the combination of Calvignac/Kloth discloses the packet processor is further configured to: maintain a bit to represent availability of the memory

entry (Kloth, col. 6, lines 6-16; Table 1; Calvignac, paragraphs 0021 and 0026; Fig. 1, element 102). *See the rejection of claims 3 and 13 above.*

19. **As per claim 29**, the combination of Calvignac/Kloth discloses the network processor is further configured to maintain a bit to represent availability of the memory entry (Kloth, col. 6, lines 6-16; Table 1; Calvignac, paragraphs 0021 and 0026; Fig. 1, element 102). *See the rejection of claims 3 and 13 above.*

20. **As per claim 32**, the combination of Calvignac/Kloth discloses maintaining a but in a status register to represent availability of the CAM entry to identify a local memory location (Kloth, col. 6, lines 6-16; Table 1; Fig. 1, element 26; Calvignac, paragraphs 0021 and 0026). *See the rejection of claims 3 and 13 above.*

21. Claims 2, 4, 5, 12, 14, 15, 22, 25, 28, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Dice et al. (U.S. Patent Application Publication 2003/0229766 (hereinafter "Dice").

22. **As per claims 2 and 12**, Calvignac discloses the multithreaded engine (paragraphs 0020, 0021, and 0026; Fig. 2, element 103).

Calvignac does not disclose maintaining a count of threads that use the memory entry.

Dice discloses maintaining a count of threads that use the memory entry (paragraph 0097).

Calvignac and Dice are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Dice's Reference-Count to Calvignac's CAM because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of improved memory management.

Therefore, it would have been obvious to combine Calvignac and Dice for the benefit of obtaining the invention as specified in claims 2 and 12.

23. **As per claims 4 and 14**, the combination of Calvignac/Dice discloses maintaining the count includes incrementing the count to represent a thread initiating use of the memory entry (Dice, paragraph 0097).

24. **As per claims 5 and 15**, the combination of Calvignac/Dice discloses maintaining the count includes decrementing the count to represent a thread halting use of the memory entry (Dice, paragraph 0097).

25. **As per claim 22**, the combination of Calvignac/Dice discloses a process to maintain a count of threads included in the multithreaded engine that use the memory entry (Dice, paragraph 0097; Calvignac, paragraphs 0020, 0021, and 0026; Fig. 2, element 103). *See the rejection of claims 2 and 12 above.*

26. **As per claim 25**, the combination of Calvignac/Dice discloses the packet processor is further capable of: maintaining a count of threads included in the multithreaded engine that use the memory entry (Dice, paragraph 0097; Calvignac,

paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, element 103). *See the rejection of claims 2 and 12 above.*

27. **As per claim 28**, the combination of Calvignac/Dice discloses the network processor is further capable of maintaining a count of threads included in the multithreaded engine that use the memory entry (Dice, paragraph 0097; Calvignac, paragraphs 0020, 0021, and 0026; Fig. 1, element 102; Fig. 2, element 103). *See the rejection of claims 2 and 12 above.*

28. **As per claim 31**, the combination of Calvignac/Dice discloses maintaining a count of threads included in the multithreaded microengine that use the CAM entry (Dice, paragraph 0097; Calvignac, paragraphs 0020, 0021, and 0026; Fig. 2, element 103).

Response to Arguments

29. Applicant's arguments with respect to **claims 1-37** in the Appeal Brief dated May 8, 2008 have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-37** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,862,674 (Dice et al.) corresponds to U.S. Patent Application Publication 2003/0229766.

2. U.S. Patent 7,167,471 (Calvignac et al.) corresponds to U.S. Patent Application Publication 2003/00448785.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
July 24, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185